AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A system for hardening a logic circuit against at least one of a single-event upset and single-event transient condition, the system comprising in combination:

a logic circuit outputting independently-obtained first and second redundant signals;

first and second feed-forward devices, wherein each of the first and second feed-forward devices is operable to receive both of the first and second redundant signals, and wherein when the first and second redundant signals are in expected states, then (i) the first feed-forward device responsively provides a first feed-forward signal and (ii) the second feed-forward device responsively provides a second feed-forward signal~~; and~~ , and wherein when at least one of the first and second redundant signals is in an unexpected state, then both the first and second feed-forward devices continue to provide their respective feed-forward signals consistent with the last expected state of the redundant signals; and

first and second feedback devices, wherein each of the first and second feedback devices is operable to receive both of the first and second feed-forward signals, and wherein when the first and second feed-forward signals are in expected states, (i) the first feedback device responsively feeds a first feedback signal back to the first redundant signal and (ii) the second feedback device responsively feeds a second feedback signal back to the second redundant signal~~.~~ , and wherein when at least one of the first and second feed-forward signals is in an unexpected state, then both the

first and second feedback devices continue to provide their respective feedback signals consistent with the last expected state of the feed-forward signals.

2. (Canceled)

3. (Currently Amended) The system of claim ~~2~~ 1, wherein at least one of the first and second redundant signals is in the unexpected state as a result of ~~an~~ a radiation-particle intrusion.

4. (Currently Amended) The system of claim ~~2~~ 1, wherein the unexpected state is propagated by any of the logic circuit, the first and second redundant signals, and the first and second feedback modules.

5. (Canceled)

6. (Currently Amended) The system of claim ~~5~~ 1, wherein at least one of the first and second feed-forward signal is in the unexpected state as a result of ~~an~~ a radiation-particle intrusion.

7. (Currently Amended) The system of claim ~~5~~ 1, wherein the unexpected state occurs in any of the logic circuit, the first and second redundant signals, the first and second feed-forward modules, and the first and second feed-forward signals.

8. (Original) The system of claim 1, wherein any of the logic circuit, first and second feed-forward devices, and first and second feedback devices comprise radiation-particle-hardened circuitry.

9. (Original) The system of claim 1, wherein any of the logic circuit, first and second feed-forward devices, and first and second feedback devices are operable to receive respective enable signals, and wherein the respective enable signals allow (i) the logic

circuit to provide a current state of the first and second redundant signals, (ii) the first and second feed-forward devices to provide a current state of their respective first and second feed-forward signals, and (iii) the first and second feedback devices to provide a current state of their respective first and second feedback signals.

10. (Original) The system of claim 9, wherein the current state comprises any of a high state, a low state, and a floating state.

11. (Original) The system of claim 9, further including a clocking circuit to provide the respective enable signals.

12. (Original) The system of claim 11, wherein the clocking circuit comprises radiation-particle-hardened circuitry.

13. (Original) The system of claim 1, wherein any of the logic circuit, first and second feed-forward devices, and first and second feedback devices are operable to receive respective enable and complementary signals, and wherein the respective enable and complementary signals allow (i) the logic circuit to provide a current state of the first and second redundant signals, (ii) the first and second feed-forward devices to provide a current state of their respective first and second feed-forward signals, and (iii) the first and second feedback devices to provide a current state of their respective first and second feedback signals.

14. (Original) The system of claim 13, wherein the current state comprises any of a high state, a low state, and a floating state.

15. (Original) The system of claim 13, further including a clocking circuit to provide the respective enable and complementary signals.

16. (Original) The system of claim 1, wherein the logic circuit, first and second feed-forward devices, and first and second feedback devices are fabricated using a bulk silicon technology.

17. (Original) The system of claim 1, wherein the logic circuit, first and second feed-forward devices, and first and second feedback devices are fabricated using a device-insulating technology.

18. (Original) The system of claim 17, wherein the device-insulating technology comprises a silicon-on-insulator technology.

19. (Currently Amended) The system of claim 1, wherein the logic circuit comprises first and second logic gates, wherein each of the first and second logic gates has (i) at least one input for receiving a desired input signal and (ii) an output for producing its redundant signal.

20. (Original) The system of claim 19, wherein the first and second logic gates comprise radiation-particle-hardened circuitry

21. (Currently Amended) The system of claim 19, wherein the logic circuit is fabricated according to a tri-rail system having a common rail operable to provide a first potential, and first and second adjacent rails operable to provide a second potential, wherein the first logic gate is formed between the first adjacent rail and the common rail, and wherein the second logic gate is formed between the second adjacent rail and the common rail.

22. (Original) The system of claim 21, wherein the first gate is physically offset from the second gate so as to prevent a single particle from passing through both gates and causing both to experience a single event upset condition.

23. (Original) The system of claim 19, wherein each of the first and second gates further include at least one input for receiving an enable signal, and wherein the enable signal allows each of the first and second gates to provide a current state of its respective redundant signal.

24. (Original) The system of claim 21, wherein the current state of the respective redundant signals comprises any of a high state, a low state, and a floating state.

25. (Currently Amended) The system of claim 19, wherein each of the first and second logic gates further include at least two inputs for receiving enable and complementary signals, and wherein the enable and complementary signals allow each of the first and second logic gates to provide a current state of its respective redundant signal.

26. (Original) The system of claim 25, wherein the current state of the respective redundant signals comprises any of a high state, a low state, and a floating state.

27. (Original) The system of claim 25, further including a clocking circuit to provide the enable and complementary signals.

28. (Original) The system of claim 27, wherein the clocking circuit includes first and second clocking modules, wherein the first clocking module is operable to provide to the first gate independently-obtained first enable and complementary signals, wherein the

second clocking module is operable to provide to the second gate independently-obtained second enable and complementary signals.

29. (Original) The system of claim 28, wherein the first and second clocking modules are physically offset from each other to prevent a single particle from passing through both clock modules and causing both to experience a single event upset condition.

30. (Original) The system of claim 28, wherein the clocking circuit is fabricated according to a tri-rail system having a common rail operable to provide a first potential, and first and second adjacent rails operable to provide a second potential, wherein the first clocking module is formed between the first adjacent rail and the common rail, and wherein the second clocking module is formed between the second adjacent rail and the common rail.

31. (Original) The system of claim 30, wherein the first clock module is physically offset from the second clocking module so as to prevent a single particle from passing through both clock modules and causing both to experience a single event upset condition.

32. (Original) The system of claim 1, wherein the first feed-forward device comprises at least one logic gate, wherein the at least one logic gate has (i) at least two inputs, and (ii) an output for producing its feed forward signal, wherein one of the inputs is operable to receive the first redundant signal, and wherein another of the inputs is operable to receive the second redundant signal.

33. (Original) The system of claim 32, wherein the at least one logic gate comprises radiation-particle-hardened circuitry.

34. (Original) The system of claim 32, wherein the first feed-forward device is fabricated according to a tri-rail system having a common rail operable to provide a first potential, and first and second adjacent rails operable to provide a second potential, wherein the at least one logic gate is formed between the first adjacent rail and the common rail.

35. (Canceled)

36. (Currently Amended) The system of claim 1, wherein the second feed-forward device comprises ~~first and second logic gates~~ at least one logic gate, , wherein ~~each the first and second gates~~ the at least one logic gate has (i) at least two inputs, and (ii) an output for producing its feed forward signal, wherein one of the inputs is operable to receive the first redundant signal, and wherein another of the inputs is operable to receive the second redundant signal.

37. (Original) The system of claim 36, wherein the at least one logic gate comprises radiation-particle-hardened circuitry

38. (Original) The system of claim 36, wherein the second feed-forward device is fabricated according to a tri-rail system having a common rail operable to provide a first potential, and first and second adjacent rails operable to provide a second potential, wherein the at least one logic gate is formed between the first adjacent rail and the common rail.

39. (Canceled)

40. (Currently Amended) The system of claim 1, wherein the first feedback device comprises at least one logic gate, wherein the at least one logic gate has (i) at least two inputs, and (ii) an output for producing its feedback signal, wherein one of the inputs is

operable to receive the first feed-forward signal, and wherein another of the inputs is operable to receive the second feed-forward signal.

41. (Original) The system of claim 40, wherein the at least one logic gate comprises radiation-particle-hardened circuitry

42. (Original) The system of claim 40, wherein the first feedback device is fabricated according to a tri-rail system having a common rail operable to provide a first potential and first and second adjacent rails operable to provide a second potential, wherein the at least one logic gate is formed between the first adjacent rail and the common rail.

43. (Canceled)

44. (Original) The system of claim 1, wherein the second feedback device comprises at least one logic gate, wherein the at least one logic gate has (i) at least two inputs, and (ii) an output for producing its feedback signal, wherein one of the inputs is operable to receive the first feed-forward signal, and wherein another of the inputs is operable to receive the second feed-forward signal.

45. (Original) The system of claim 40, wherein the at least one logic gate comprises radiation-particle-hardened circuitry.

46. (Original) The system of claim 40, wherein the second feedback device is fabricated according to a tri-rail system having a common rail operable to provide a first potential and first and second adjacent rails operable to provide a second potential, wherein the at least one logic gate is formed between the first adjacent rail and the common rail.

47. (Original) The system of claim 40, wherein the second feedback device is fabricated according to a tri-rail system having a common rail operable to provide a first potential

and first and second adjacent rails operable to provide a second potential, wherein the at least one logic gate is formed between the second adjacent rail and the common rail.

48. (Original) A system for hardening a logic circuit against at least one of a single-event upset and single-event transient condition, the system comprising in combination:

first and second tristate inverters, wherein responsive to a desired input signal, the first and second tristate inverters are operable to provide respective first and second redundant signals, and wherein the first and second redundant signals are in an expected state;

first and second feed-forward-tristate inverters, wherein each the first and second feed-forward-tristate inverters is operable to receive both of the first and second redundant signals, and wherein when both of the first and second redundant signals are in the expected state, then (i) the first feed-forward-tristate inverter responsively provides a first feed-forward signal having a state complementary to the expected state and (ii) the second feed-forward device responsively provides a second feed-forward signal having a state complementary to the expected state; and

first and second feedback-tristate inverters, wherein each of the first and second feedback-tristate inverters is operable to receive both of the first and second feed-forward signals, and wherein when both the first and second feed-forward signals are in the complementary state, then (i) the first feedback-tristate inverter responsively feeds back to the first redundant signal a first feedback signal having the same state as the expected state of the first redundant signal and (ii) the second feedback device responsively feeds back to the second redundant signal a second feedback signal having the same state as the expected state of the second redundant signal.

49. (Original) The system of claim 48, wherein when at least one of the first and second redundant signals is in an unexpected state, then at least one of the first and second feed-forward-tristate inverters floats its output so as to not propagate the unexpected state of the redundant signals and instead maintains the expected state of the respective feed-forward signal.

50. (Original) The system of claim 49, wherein at least one of the first and second redundant signals is in the unexpected state as a result of an radiation-particle intrusion.

51. (Original) The system of claim 50, wherein the unexpected state is propagated by any of the first and second tristate inverters, the first and second redundant signals, and the first and second feedback-tristate inverters.

52. (Original) The system of claim 48, wherein when at least one of the first and second feed-forward signals is in an unexpected state, then at least one of the first and second feedback-tristate inverters floats its output so as to not propagate the unexpected state of the feed-forward signals and instead maintains the expected state of the respective feed-back signal.

53. (Original) The system of claim 52, wherein at least one of the first and second feed-forward signal is in the unexpected state as a result of an radiation-particle intrusion.

54. (Original) The system of claim 52, wherein the unexpected state is propagated by any of the first and second tristate inverters, the first and second redundant signals, the first and second feed-forward-tristate inverters, and the first and second feed-forward signals.

55. (Original) The system of claim 48, wherein each of the first and second tristate inverters, first and second feed-forward-tristate inverters, and first and second feedback-tristate inverters comprises at least one radiation-particle-hardened-tristate inverter.

56. (Canceled)

57. (Original) A method for hardening a logic circuit against at least one of a single-event upset and single-event transient condition, the method comprising in combination:

providing to first and second feed-forward devices independently-obtained first and second redundant signals, wherein the first redundant signal is in an expected state and the second redundant signal is in an unexpected state;

providing to first and second feedback devices a first feed-forward signal as a function of logic operation on both of the first and second redundant signals, wherein the logic operation is operable to not change a current state of the first feed-forward signal;

providing to first and second feedback devices a second feed-forward signal as a function of logic operation on both of the first and second redundant signals, wherein the logic operation is operable to not change a current state of the second feed-forward signal;

providing to the first redundant signal a first feedback signal as a function of logic operation on both of the first and second feed-forward signals, wherein the logic operation is operable to not change a current state of the first feedback signal; and

providing to the second redundant signal a second feedback signal as a function of logic operation on both of the first and second feed-forward signals, wherein the logic operation is operable to not change a current state of the second feedback signal.

58. (Original) A method for hardening a logic circuit against at least one of a single-event upset and single-event transient condition, the method comprising in combination:

providing to first and second feed-forward devices independently-obtained first and second redundant signals, wherein the first redundant signal in an unexpected state and the second redundant signal in an expected state;

providing to first and second feedback devices a first feed-forward signal as a function of logic operation on both of the first and second redundant signals, wherein the logic operation is operable to not change a current state of the first feed-forward signal;

providing to first and second feedback devices a second feed-forward signal as a function of logic operation on both of the first and second redundant signals, wherein the logic operation is operable to not change a current state of the second feed-forward signal;

providing to the first redundant signal a first feedback signal as a function of logic operation on both of the first and second feed-forward signals, wherein the logic operation is operable to not change a current state of the first feedback signal; and

providing to the second redundant signal a second feedback signal as a function of logic operation on both of the first and second feed-forward signals, wherein the logic operation is operable to not change a current state of the second feedback signal.

59. (Original) A method for hardening a logic circuit against at least one of a single-event upset and single-event transient condition, the method comprising in combination:

providing to first and second feed-forward devices independently-obtained first and second redundant signals as a function of logic operation on a desired input

signal, wherein the logic operation is operable to provide the first and second redundant signals in first expected states;

providing to first and second feedback devices a first feed-forward signal in an unexpected state;

providing to first and second feedback devices a second feed-forward signal as a function of logic operation on both of the first and second redundant signals, wherein the logic operation is operable to provide the second feed-forward signal in a second expected state;

providing to the first redundant signal a first feedback signal as a function of logic operation on both of the first and second feed-forward signals, wherein the logic operation is operable to not change a current state of the first feedback signal; and

providing to the second redundant signal a second feedback signal as a function of logic operation on both of the first and second feed-forward signals, wherein the logic operation is operable to not change a current state of the second feedback signal.

60. (Original) A method for hardening a logic circuit against at least one of a single-event upset and single-event transient condition, the method comprising in combination:

providing to first and second feed-forward devices independently-obtained first and second redundant signals as a function of logic operation on a desired input signal, wherein the logic operation is operable to provide the first and second redundant signals in first expected states;

providing to first and second feedback devices a first feed-forward signal as a function of logic operation on both of the first and second redundant signals, wherein

the logic operation is operable to provide the first feed-forward signal in a second expected state;

providing to first and second feedback devices a second feed-forward signal in an unexpected state;

providing to the first redundant signal a first feedback signal as a function of logic operation on both of the first and second feed-forward signals, wherein the logic operation is operable to not change a current state of the first feedback signal; and

providing to the second redundant signal a second feedback signal as a function of logic operation on both of the first and second feed-forward signals, wherein the logic operation is operable to not change a current state of the second feedback signal.